A 50nm Depleted-Substrate CMOS Transistor (DST)

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I. Abstract

In this paper we show a Depleted-Substrate Transistor (DST) technology which demonstrates significant performance gain over bulk Si transistors without the floating body effect (FBE). We have fabricated depleted-substrate CMOS transistors on thin silicon body (≤30nm) with physical gate lengths down to 50nm which show much steeper subthreshold slopes (≤ 75mV/decade) and improved DIBL (≤50mV/V) over both partially-depleted (P-D) SOI and bulk Si, for both PMOS and NMOS transistors. The salicide formation and high parasitic resistance problems associated with the use of thin Si body can be overcome by using raised source/drain. Depleted-substrate PMOS transistors with 50nm physical gate length and raised source/drain were fabricated and achieved I_{on} = 0.65mA/um and I_{off} = 9nA/um at V_{cc} = 1.3V. This PMOS drive current is the highest ever reported, and is about 30% higher than any previously published PMOS I_{on} value for both PD-SOI and bulk Si at a given I_{off}. The use of raised source/drain improved the I_{on} of the depleted-substrate NMOS transistors by ~20%. Depleted-substrate NMOS transistors with 65nm physical gate length and raised source/drain achieved DIBL = 45mV/V, subthreshold slope = 75mV/decade, I_{on} = 1.18mA/um and I_{off} = 60nA/um at V_{cc} = 1.3V, as well as significant improvement in Id-Vd characteristics due to a 60% reduction in DIBL and >25% improvement in subthreshold slope over the bulk Si.

II. Introduction

There are two kinds of planar SOI transistor structures, namely the partially-depleted (P-D) SOI and fully-depleted (F-D) SOI. Previously we evaluated P-D SOI CMOS transistors and concluded that P-D SOI has diminishing performance gain with scaling over standard bulk Si CMOS [1, 2]. In addition, standard P-D SOI transistors exhibit FBE which puts a significant burden on circuit design. On the other hand, it is well-known that fully-depleted (F-D) SOI transistors eliminate the FBE while providing better subthreshold slopes than bulk Si transistors [3-5]. However, there are very few reports on F-D SOI transistors with physical gate lengths less than 100nm, and the scalability of F-D SOI technology is unknown. In this paper we evaluate a thin-silicon-body depleted-substrate transistor technology with a focus on sub-70nm physical gate lengths and examine its scalability and performance down to 50nm. We give this transistor technology a generic name of Depleted-Substrate Transistor (DST).

III. Process

Sub-70nm depleted-substrate CMOS transistors were fabricated on thin silicon body with thickness ≤ 30nm on top of a ~200nm buried oxide. The physical gate oxide thickness was equal to 1.5nm. Figure 1 shows a TEM cross section of a thin-silicon-body depleted-substrate transistor. To overcome the salicide formation and high parasitic resistance problems in thin-silicon-body devices, raised source/drain can be used. Figure 2 shows a TEM cross section of the DST with raised source/drain. In this experiment depleted-substrate transistors with and without raised source/drain were fabricated down to 50nm. Standard 0.13um-generation CMOS transistors with ~70nm physical gate length and 1.5nm physical gate oxide [6] were used as the control.

IV. Device Characteristics and Discussion

Figures 3 and 4 show the subthreshold Id-Vg characteristics of the 70nm depleted-substrate PMOS and NMOS transistors respectively without raised source/drain. Included are the standard bulk Si transistors for reference. Both the PMOS and NMOS show steeper subthreshold slopes (≤ 75mV/decade) and reduced DIBL (≤50mV/V) compared to the control. Figures 5 and 6 show the Id-Vd family of curves for PMOS and NMOS respectively. There are no abnormal subthreshold slope changes or kink-effects, indicating the absence of FBE. The PMOS and NMOS inversion CV curves are shown in Figure 7. The results show no abnormality in forming ultra-thin gate oxide on the thin Si body. Figure 8 shows the channel mobility of the thin-Si-body DST and the bulk Si transistor. The data shows no channel mobility degradation in the thin Si body.

To improve salicide formation and reduce parasitic resistances on thin-silicon-body devices, raised source/drain technique can be used. Figure 9 shows the Id-Vg characteristics of a depleted-substrate PMOS transistor with 50nm physical gate length and raised source/drain. It achieves DIBL = 40mV/V, subthreshold slope = 70mV/decade, I_{on} = 0.65mA/um and I_{off} = 9nA/um at V_{cc} = 1.3V. This is the highest PMOS I_{on} value ever reported for a given I_{off}, and is ~30% higher than any previously published PMOS I_{on} value for both P-D SOI and bulk Si at a given I_{off} [6]. Figure 10 shows the Id-Vd family of curves for this 50nm PMOS transistor. Figure 11 shows the PMOS I_{on}-I_{off} comparison of the depleted-substrate transistor, the depleted-substrate transistor with raised source/drain and the standard 0.13um-generation bulk Si transistors at V_{cc} = 1.3V. For a given I_{off} (e.g. 1.0 nA/um), the depleted-substrate transistor with raised source/drain shows the highest I_{on} value, about 30% higher than the standard bulk Si transistor. Figure 12 shows that compared to the standard Si bulk PMOS at 1.3V, depleted-substrate PMOS with raised source/drain is able to achieve the same I_{on}-I_{off} performance at 1.1V and reduces the power by at least 30% (power α voltage^2).

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The use of raised source/drain also improves salicide formation and reduces the parasitic resistance problems in the case of the depleted-substrate NMOS transistor. Figure 13 shows the I_{on}-I_{off} comparison of the NMOS DST with versus without raised source/drain. The data shows that for a given I_{off}, raised source/drain improves I_{on} of the NMOS DST by ~20%. This I_{on} improvement can be increased by further optimizing the raised source/drain formation and reducing parasitic resistances. Figures 14 and 15 compare the Id-Vg and Id-Vd characteristics respectively of the NMOS DST transistor with raised source/drain and the bulk Si control. Both transistors have physical gate length of 65nm. The results show that compared to the bulk Si control, the DST shows significant device performance improvement. Figure 14 shows that the DST NMOS achieves DIBL = 45mV/V, subthreshold slope = 75mV/decade, I_{on} = 1.18mA/um and I_{off} = 60nA/um at V_{cc} = 1.3V (this I_{on} can be increased by further optimizing the raised source/drain formation). Figure 15 shows the much improved Id-Vd characteristics of the NMOS DST due to the 60% reduction in DIBL and >25% improvement in subthreshold slope over the bulk Si control.

V. Summary

We have shown here depleted-substrate transistor (DST) technology on thin-Si-body can be scaled to 50nm physical gate length with significant performance gain over bulk Si without FBE. Sub-70nm depleted-substrate CMOS transistors were fabricated on thin silicon body (≤ 30nm) and shown to have much steeper subthreshold slopes (≤ 75mV/decade), reduced DIBL (≤ 50mV/V), similar CV characteristics and channel mobility compared to standard bulk Si CMOS transistors, for both PMOS and NMOS. 50nm physical-gate-length depleted-substrate PMOS transistors with raised source/drain achieved I_{on} = 0.65mA/um and I_{off} = 9nA/um at V_{cc} = 1.3V. This is the highest PMOS drive current ever reported for a given I_{off}, and is ~30% higher than any previously published PMOS I_{on} value for both P-D SOI and bulk Si at a given I_{off}. The use of raised source/drain improved the I_{on} of the depleted-substrate NMOS transistors by ~20%. Depleted-substrate NMOS transistors with 65nm physical gate length and raised source/drain achieve DIBL = 45mV/V, subthreshold slope = 75mVdecade, I_{on} = 1.18mA/um and I_{off} = 60nA/um at V_{cc} = 1.3V, as well as much improved Id-Vd characteristics due to the 60% reduction in DIBL and >25% improvement in subthreshold slope over the bulk Si.

VI. Acknowledgements

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VII. References

[1] R. Chau et al., IEDM Tech. Digest, pp. 591-594, 1997.
[2] K. Mistry et al., Symp. VLSI Tech. Digest, pp. 204-205, 2000.
[3] Y.-K. Choi et al., Symp. VLSI Tech. Digest, pp. 19-20, 2001.
[4] T. Ohno et al., Symp. VLSI Tech. Digest, pp. 25-26, 1993
[5] D. Hisamoto et al., Symp. VLSI Tech. Digest, pp. 208-209, 2000.
[6] S. Tyagi et al., IEDM Tech. Digest, pp. 567-570, 2000.

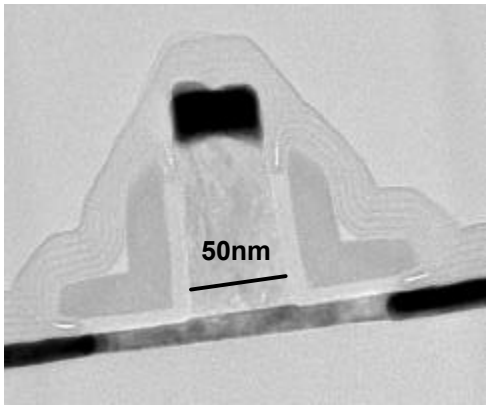

Fig.1. TEM cross-section of a depleted-substrate transistor (DST) on thin silicon body.

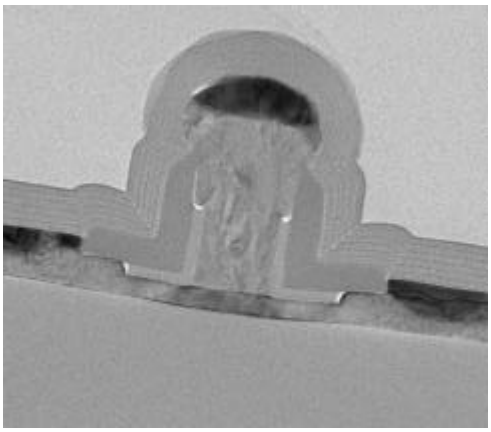

Fig.2. TEM cross-section of a raised-source/drain depleted-substrate transistor (DST) on thin silicon body.

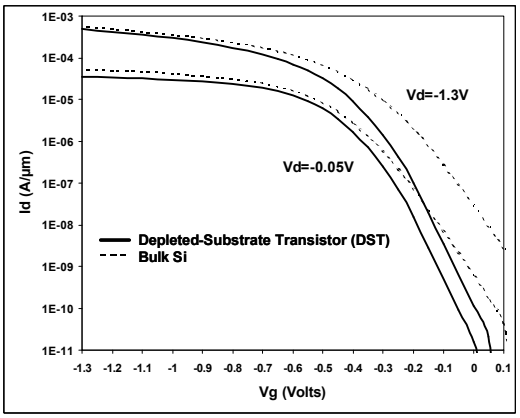

Fig. 3. Subthreshold Id-Vg characteristics of the 70nm depleted-substrate PMOS (without raised source/drain) and bulk Si PMOS.

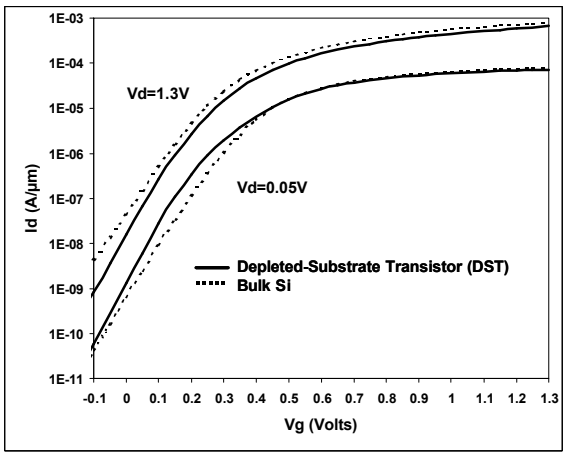

Fig. 4. Subthreshold Id-Vg characteristics of the 70nm depleted-substrate NMOS (without raised source/drain) and bulk Si NMOS.

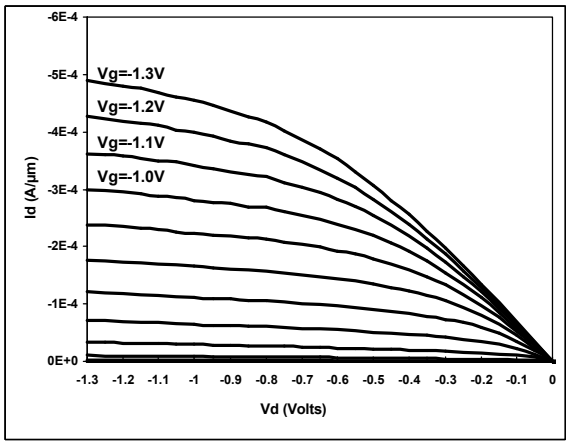

Fig. 5. Id-Vd family of curves for the 70nm depleted-substrate PMOS (without raised source/drain).

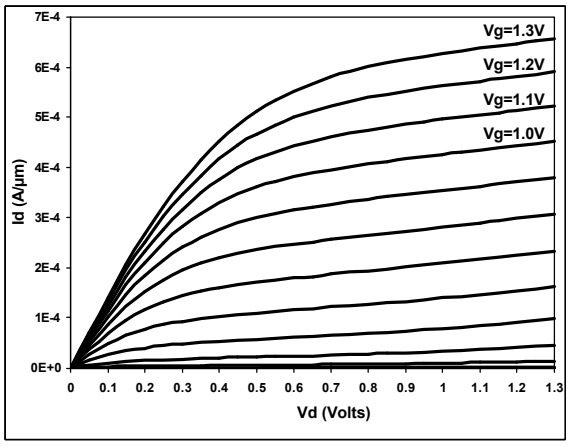

Fig. 6. Id-Vd family of curves for the 70nm depleted-substrate NMOS (without raised source/drain).

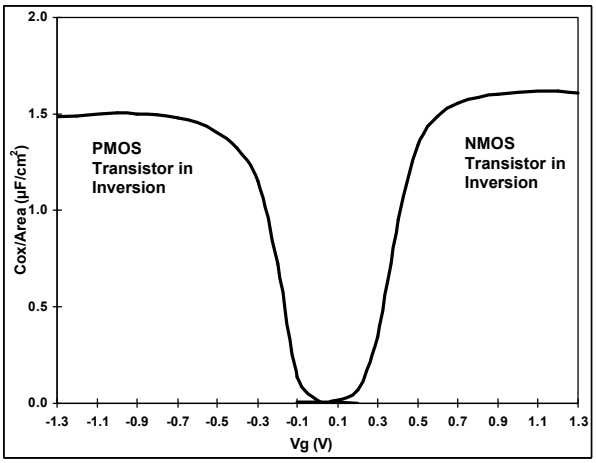

Fig. 7. PMOS and NMOS inversion C-V plots for the thin-Si-body depleted-substrate transistor. Physical gate oxide thickness = 1.5nm.

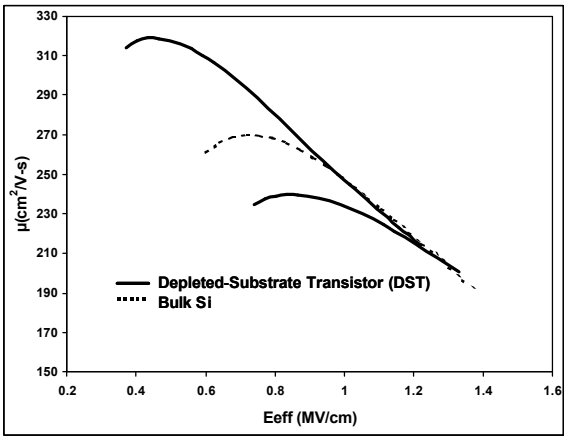

Fig. 8. NMOS channel mobility of high and low Vt thin-Si-body depleted-substrate transistor versus bulk Si transistor.

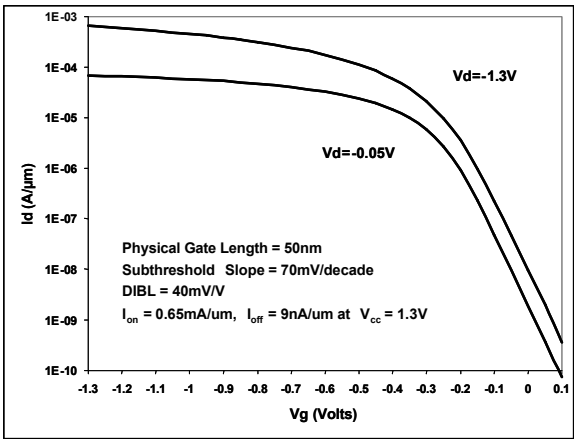

Fig. 9. Subthreshold Id-Vg characteristics of the 50nm physical-gate-length depleted-substrate PMOS transistor with raised source/drain.

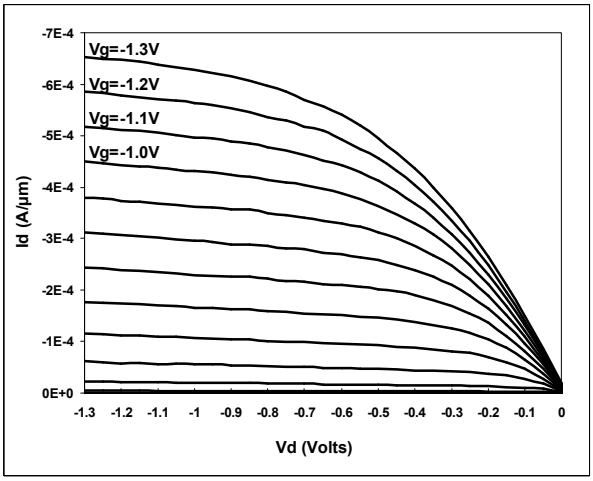

Fig. 10. Id-Vd family of curves for the 50nm physical-gate-length depleted-substrate PMOS with raised source/drain.

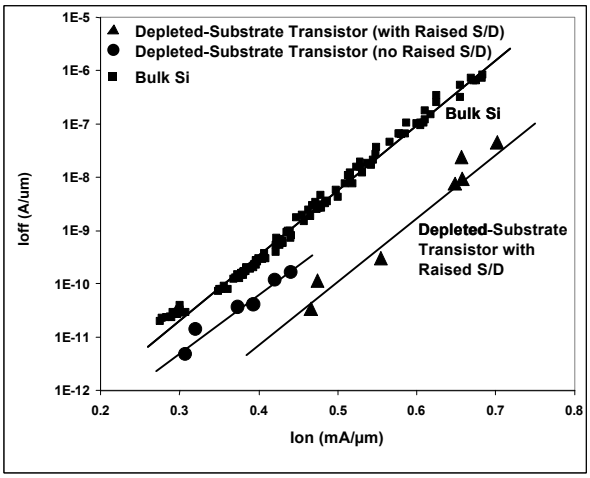

Fig. 11. PMOS I_{on}-I_{off} comparison of the depleted-substrate transistor (no raised source/drain), the depleted-substrate transistor with raised source/drain, and the standard 0.13um-generation bulk Si transistor at V_{cc} = 1.3V.

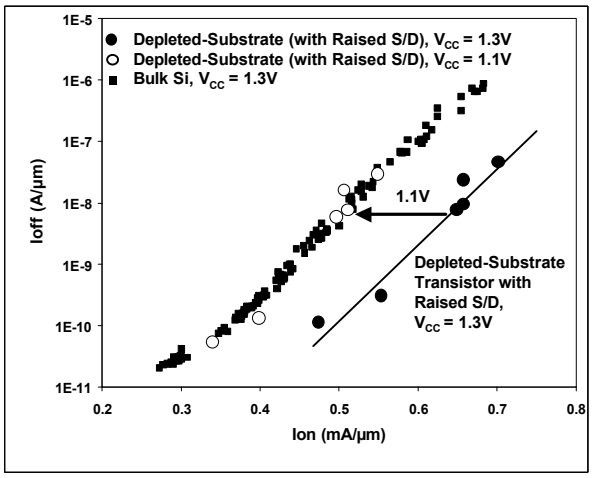

Fig. 12. DST PMOS (with raised S/D) at 1.1V achieves identical I_{on}-I_{off} performance to bulk Si PMOS at 1.3V, with ~30% power reduction.

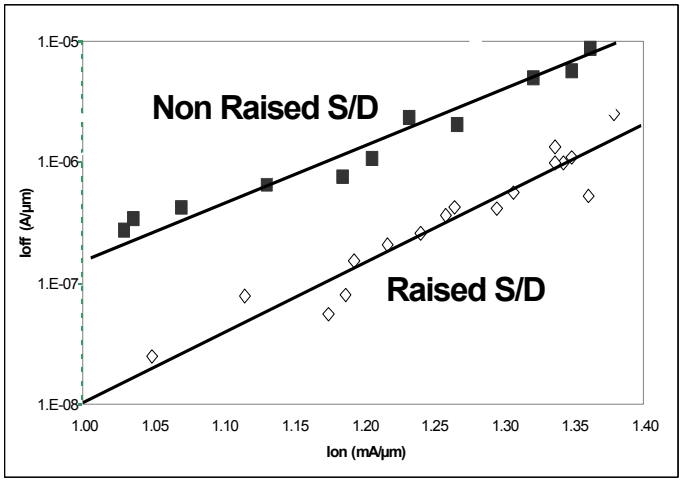

Fig. 13. NMOS I_{on}-I_{off} comparison of the depleted-substrate transistor (no raised source/drain) and the depleted-substrate transistor with raised source/drain at V_{cc} = 1.3V.

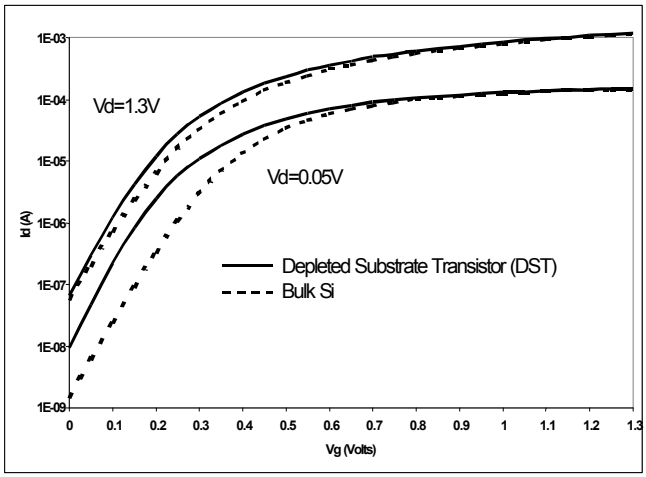

Fig. 14. Subthreshold Id-Vg characteristics of the 65nm physical-gate-length depleted -substrate NMOS (with raised source/drain) and bulk Si NMOS.

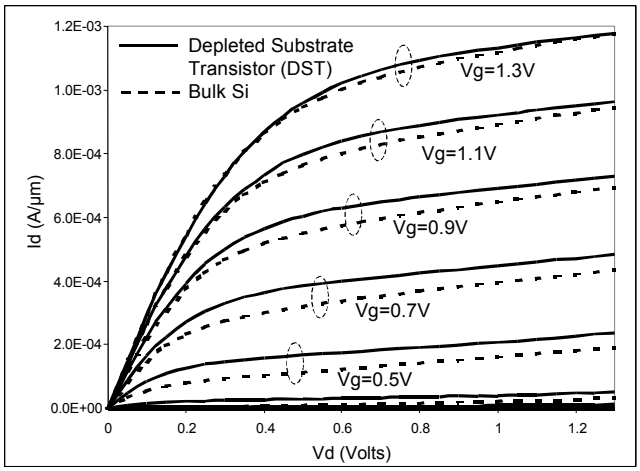

Fig. 15. Id-Vd characteristics of the 65nm depleted-substrate NMOS (with raised source/drain) and bulk Si NMOS.